Q.P. Code: 18CS0502 **R18**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech I Year II Semester Supplementary Examinations October-2020

DIGITAL LOGIC DESIGN

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

PART-A

(Answer all the Questions **5 x 2 = 10** Marks)

1	**a**	Explain about Diminished Radix complement.	**2M**
	b	Define Min-term & Max-term.	**2M**
	c	Explain Applications of Multiplexer.	**2M**
	d	Define Race Around Condition.	**2M**
	e	What is Cache Memory?	**2M**

PART-B

(Answer all Five Units 5 x 10 = 50 Marks)

UNIT-I

2		Explain the Binary codes with examples.	**10M**
		OR	
3	**a**	Explain binary to Gray & Gray to binary conversion with example.	**5M**
	b	State and Explain the DeMorgan's Theorem and Consensus Theorem.	**5M**

UNIT-II

4		Reduce the expression f(x,y,z,w)= πM(0,2,7,8,9,10,11,15) .d (3,4) using K-Map.	**10M**
		OR	
5		Obtain the a) SOP b) POS expression for the function given below F(A,B,C,D) = Σm(0,1,2,5,8,9,10)	**10M**

UNIT-III

6	**a**	Design a 4 bit binary parallel subtractor and the explain operation in detail.	**5M**
	b	Design the combinational circuit of 4 Bit Parallel Adder.	**5M**
		OR	
7		Design a combinational circuit for converting binary code to gray code.	**10M**

UNIT-IV

8	**a**	Explain the Logic diagram of master-slave JK flip-flop.	**5M**
	b	Write difference between Combinational & Sequential circuits.	**5M**
		OR	
9	**a**	Draw and explain the operation of SR LATCH?	**5M**
	b	Explain about Ring counter.	**5M**

UNIT-V

10		Design PAL for a combinational circuit that squares a 3-bit number.	**10M**
		OR	
11	**a**	Explain about TTL family.	**5M**
	b	Explain about memory decoding error detection and correction.	**5M**

END